Course Type	Course Code	Name of Course	L	T	P	Credit
DE	NCSD517	**VLSI Design and Testing**	3	0	0	3

Course Objective

At the end of the course, the students will be able to

- know IC fabrication methods.
- express the Layout of simple MOS circuit using Lambda based design rules.
- develop some algorithms for VLSI Design.
- familiar with testing issues in VLSI
- develop some algorithms for VLSI testing.

Learning Outcomes

The main objective of this course is

- to provide in-depth knowledge on VLSI Design methodologies and Testing.
- to provide knowledge of verilog coding and some graph algorithms for physical design.
- to understand the problems encountered in testing large circuits, approaches to detect and diagnose the faults and methods to improve the design to make it testable.

Unit No.	Topics to be Covered	Lecture Hour	Learning Outcome
1	Introduction to VLSI Design, MOS logic: nMOS, pMOS and CMOS	2	To learn basic concepts of MOS logic.
2	MOS inverter, stick diagram, design rules and layout, delay analysis.	2	Students gain the knowledge about Layout design and delay.
3	ASIC Library Design: Transistors as Resistors and parasitic Capacitance, Logical effort, gate array, standard cell and data path cell design.	3	Students gain the knowledge about ASIC library design
4	Some graph algorithms for physical design	4	Since, graphs are used to model many VLSI physical design so student will learn various graphs algorithms which are used in modelling of physical design problems.
5	Introduction to hardware description language (HDL) Verilog/VHDL.	4	Students get familiar with Verilog/VHDL.
6	Test process and ATE and Test economics, Yield Analysis and product quality	2	Students gain the knowledge about Test process, Test Economics and yield analysis.
7	Fault modelling and Fault simulation	3	Student will get the idea about various fault modelling technique and fault simulation for design verification as well as test evaluation.
8	Combinational ATPG – D, PODEM, FAN	3	Students gain the basic idea of combinatitaional testing
9	Sequential ATPG- ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Simulation- Based Sequential Circuit ATPG.	6	Students gain the knowledge about sequential ATPG.
10	Built-in Self-test	6	Self-Testing Pattern Generation and Response Compaction
11	Delay test, IDDQ testing	5	Importance of IDDQ test for failure effect analysis will be understood.
12	Boundary scan	2	Student will learn issues related to area overhead and scan sequence length. Also get the idea of IEEE1149.1 architecture.
	Total	**42**	

Text Books:

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, by M. Bushnell and Viswani Agrawal, Springer, October, 2013.

Basic VLSI Design, by A. Pucknell, Prentice Hall India Learning, January, 1995

Reference Books:

Verilog HDL A guide to Digital Design and Synthesis, by Samir Palnitkar Pearson, 2003.